The Laddic — A Magnetic Device for Performing Logic

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The Laddic is a ladder-like structure cut out of a rectangular hysteresis-loop ferrite. The sides of the ladder and all of the rungs are equal in minimum cross section so that all possible paths are flux-limited. The structure presents a large number of possible flux paths. By controlling the actual switching path through the structure any Boolean function of n variables can be produced.

A number of methods of operation are discussed, and design formulae and experimental results presented. One of the attractive features of this device is that the operating currents are not critical. Therefore, it can be operated at speeds limited essentially only by the current drives available. The output may be taken during the input variable phase or during a subsequent reset phase. Switching speeds of a few tenths of a microsecond and repetition rates of a few hundred kilocycles have been achieved.

I. INTRODUCTION

Toroidal cores of magnetic material having a rectangular hysteresis loop are widely used as memory and switching elements in logic circuitry.[1] The possibility of simplifying core circuitry by using more complicated cores has occurred to a number of people, and several multihole core devices for specific applications have been described in the literature.[2, 3, 4] The present work was initiated to explore the possible systematic use of the magnetic "linkages" between flux patterns in a multihole magnetic structure. In particular, it was hoped that core circuits could be simplified by replacing the function of coupling windings between individual cores by the magnetic "linkages". A structure containing a continuous network of flux-limited paths was considered, and a generalized technique was developed for realizing any class of Boolean switching function* in combinational logic by controlling the switching

* The use of Boolean notation and algebra is described, for example, in Ref. 1.

path through the network. For specific switching functions there are a large number of geometries which can be used. In the present paper one structure that can be used generally for all combinational logic will be described. This specific structure resembles a ladder, Fig. 1, and has been named "Laddic," an abbreviation for "ladder-logic."

II. OUTLINE OF PAPER

The general principle of operation of the Laddic is discussed in Section III. Briefly, the structure shown in Fig. 1 is made out of a rectangular hysteresis loop material, for example, a memory-core ferrite. The cross sections of its rungs are all equal and the cross sections of the side rails are preferably equal to that of the rungs, but may be greater. It is found that, starting from a suitable saturation flux pattern, a drive applied so as to switch flux in the first rung will switch the flux almost entirely through the closest available rung rather than split it among all available rungs.

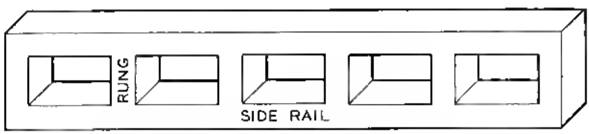

Fig. 1 — Basic Laddic structure.

In Section IV it is shown how the Laddic is used to generate Boolean functions. Briefly, the procedure is as follows. A suitable remanent flux pattern is first established by a current pulse through a reset winding. One unit of flux, corresponding to the saturation flux through one rung, is then reversed in the first rung by applying a clock-pulse current to an appropriate winding. An output winding is placed on some other rung — the last rung, for example. The reset flux pattern was such that the reversed flux preferentially chooses return paths other than through the output rung. Thus, the output is normally zero. However, if all the alternative paths are blocked by inhibiting fields produced by current pulses representing input variables, the switched flux must return through the output rung, and an output will be obtained. It will be shown that any Boolean function can be realized as the output of a single Laddic of suitable length. Of course, there are practical limitations on the size of the structure and, therefore, to the number of variables that can actually be handled. Modified circuits and modified structures will also be discussed.

In Section V some experimental results and design formulae are pre-

sented. Because all paths are flux-limited, the operating current margins in the Laddic are very broad. The variable currents must exceed a minimum value proportional to the clock current, but, practically speaking, they have no upper limit, which is a considerable advantage. Furthermore, the variable currents perform only an inhibiting function; that is, they are not required to switch flux. Thus, the back voltages induced in the variable input windings are very small, so that relatively low power sources may be used for the variable inputs. Because the input drives have no set maximum, the speed of operation is limited mainly by the abitrary maximum set for the drives. Using available materials and transistorized driving circuits, this means that switching speeds are normally in the region of 1 to 10 microseconds. The materials used are those developed for memory cores and, in general, the Laddic is compatible with core circuitry.

Section VI presents a general discussion of practical considerations.

III. PRINCIPLE OF THE LADDIC

The basic structure is that shown in Fig. 1. Three states of the material are considered. The first two are the remanent points for saturation in positive and negative senses, and correspond to the "1" and "0" states of a memory core. The third is the point of zero remanent magnetization, shown for illustration as state "2" in Fig. 2. It should be realized that

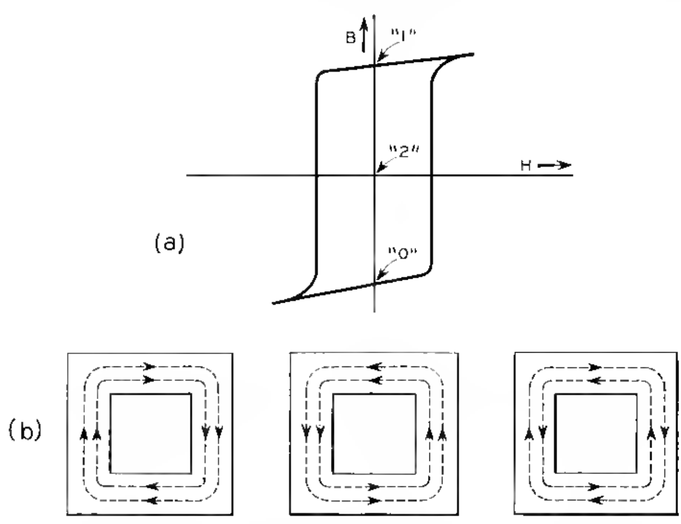

Fig. 2 — (a) Hysteresis loop showing the three states of the magnetization considered; (b) graphical representation of the three states.

state "2" is not arrived at by a sinusoidal demagnetization but by partial switching of the core from a saturated state. In the equi-flux networks being considered, a convenient model is to represent the state of magnetization of the material graphically by means of two parallel arrows, each in the direction of magnetization, and each representing one-half of the remanent saturation flux. Thus, if the arrows are in the same direction, the material is considered to be in one of the two saturated states. If they are in opposite directions, the resultant magnetization is zero and the material is considered to be in state "2". This enables one to represent the state of magnetization by closed flux patterns, as illustrated in Fig. 2(b). However, it should be kept in mind that the actual domain structure has not been observed experimentally. It is undoubtedly more complex than would follow from the simple flux patterns described, which are used solely for the purposes of a working model. Nevertheless, the model is found to be adequate for practical usage. The additional assumption that flux paths are closed within the structure, i.e., air-leakage is small, has also been found to be sufficient for the structures and materials considered.

Because of the flux-limited nature of the Laddic structure, when a reversal field is applied to the first rung the switched flux is returned

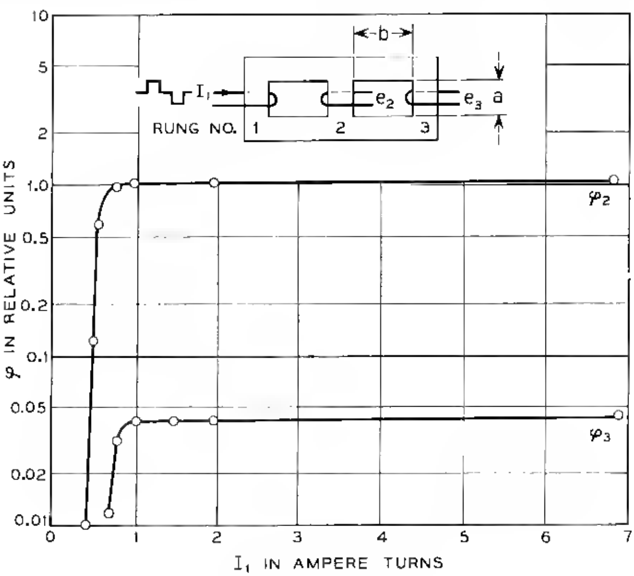

Fig. 3 — Proportions of the total flux $\varphi = \int e dt$ switched through rungs 2 and 3 by a drive applied to rung 1.

TABLE I — φ_2/φ_3 FOR DIFFERENT GEOMETRIES

	b/a		
	1	2	3.5
φ_2/φ_3	21	83	710

almost entirely through the closest available path, no matter how large the applied drive. To illustrate this, consider the three-rung Laddic shown in the inset of Fig. 3. When alternately positive and negative current pulses are applied to the winding on rung 1, flux is switched alternately up and down. The switched flux is returned via rungs 2 and 3, the flux returned through each rung being φ_2 and φ_3 respectively. Fig. 3 shows experimental values of φ_2 and φ_3 versus the applied drive I_1. It will be seen that the flux ratio φ_2/φ_3 remains virtually constant once the minimum drive current, which is necessary to produce a full reversal, is exceeded. The ratio φ_2/φ_3 depends upon the geometry factor b/a, the ratio of rung spacing to side-rail spacing, as illustrated by Table I, which gives experimental values for a manganese magnesium ferrite. These ratios are much larger than might be expected. For example, considering the case $b/a = 1$, the mmf acting on rung 2 is three times as large as that acting on rung 3. Thus, because the rate of switching in a rectangular loop ferrite is proportional to the applied field, it might be expected that φ_2/φ_3 be more nearly 3:1 at drives much larger than threshold, rather than the 21:1 found experimentally. Obviously, the flux-splitting mechanism is complicated by the dynamic magnetic reluctances of the two paths. Unfortunately, the theoretical understanding of the switching mechanism in these materials is incomplete, so that a quantitative interpretation cannot be given. The important thing is that, under these conditions, the shortest return path containing flux that can be switched acts virtually as a magnetic short circuit.

It follows that the flux paths in the three-rung Laddic for the two cases considered can be represented approximately as in Figs. 4(a) and 4(b). As discussed previously, the flux in rung 3 is represented as being in the "2" state. Clearly, this is only an approximation to the true flux pattern because, in accordance with Table I, rung 2 will not in fact be fully saturated.

It is of interest to note that the flux pattern shown in Fig. 4(c) gives the same flux distribution in the rungs as does that in Fig. 4(a). However, there is a physical difference. The flux pattern of Fig. 4(c) is that obtained following several flux reversals by a drive applied to a winding on rung 2,

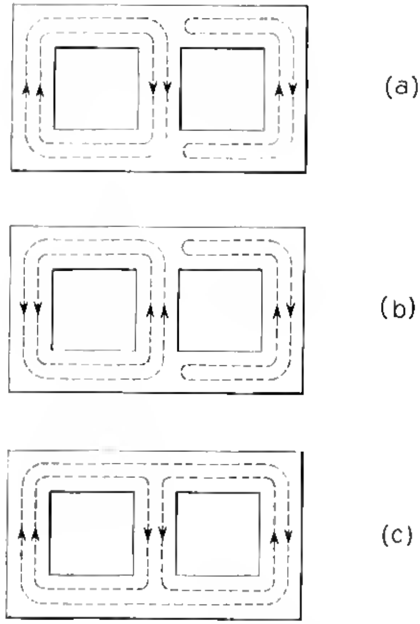

Fig. 4 — Three stable flux patterns in a three-rung Laddic.

whereas the flux pattern of Fig. 4(a) was obtained following several flux reversals by a drive applied to a winding on rung 1. If the initial flux pattern is symmetrical, as in Fig. 4(c), and a further reversal pulse is now applied to the rung 2 winding, the switched flux will divide equally between rung 1 and rung 3, as expected because of the symmetry. However, if there is a local flux closure, as in the initial flux pattern shown in Fig. 4(a), the switched flux shows a preference for the rung 1 return, so that there is a small but significant difference in the flux switched through rungs 1 and 3. This difference is small enough that it need not normally be taken into account in describing the Laddic as a device.

IV. USE OF THE LADDIC IN LOGIC CIRCUITS

4.1 *Basic Procedures*

The operation of the Laddic as an AND gate can now be explained in detail. A symmetrical flux pattern is first established by saturating odd-numbered rungs in the upward direction and even-numbered rungs in the downward direction, by pulsing a current through the reset wind-

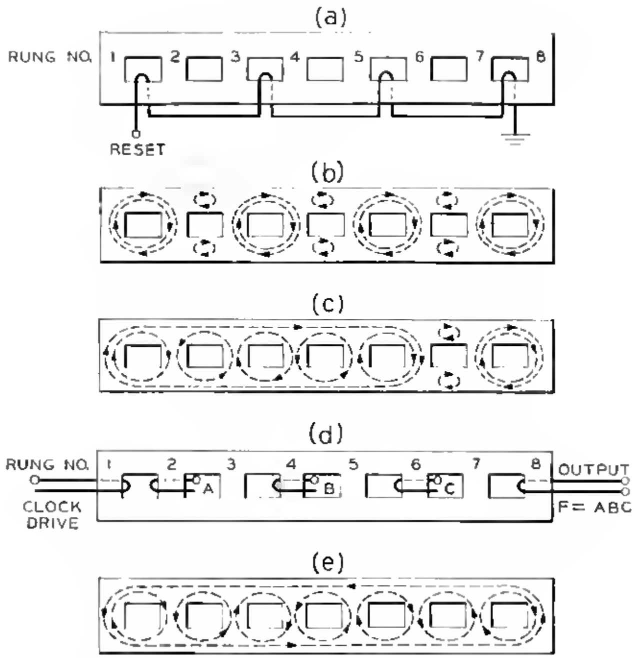

Fig. 5 — Applied drives and flux patterns for the normal mode of operation of the Laddic.

ing shown in Fig. 5(a).* The resulting flux pattern may take a number of forms, depending on the previous flux pattern. Figs. 5(b) and 5(c) illustrate two of these possibilities. The direction of magnetization of the rungs is the same in both cases, but the flux closures in the side rails are different. This difference produces only small differences in subsequent flux switching, as discussed previously, and need not be considered here.

If, following the reset, a current pulse is applied to a winding on rung 1, Fig. 5(d), in a direction to switch flux down, the flux return will be through the closest available path, i.e., through rung 2. However, if a current pulse corresponding to an input variable A is simultaneously present on rung 2, and is in a direction to hold it down, this rung is not available. Rung 3 is already saturated upwards, as are rungs 5 and 7, so these paths are also not available. Similarly, if inputs B and C are also present and hold the flux in their respective rungs, rungs 4 and 6

* The reset winding shown in Fig. 5(a) does not necessarily produce the exact flux pattern described. However, this turns out to be unimportant for normal use of the Laddic and, for simplicity, we have chosen to consider only the pattern shown. In any case, if desired, this pattern could be produced by a suitable winding.

are not available. Thus, if variables A, B and C are all present, then the return for flux switched in rung 1 must be through rung 8, and an output will result. It may be observed that the ouput voltage corresponds to a half reversal of the saturation flux, because of flux limiting by the side rail.

An output of the reverse polarity will be obtained during the subsequent reset phase; in this sense, the device also has memory.

The flux pattern obtained after a Boolean input ABC is shown in Fig. 5(e).

Obviously the "hold" currents that are necessary to prevent flux from being switched in the variable rungs, must exceed a certain minimum. However, because they serve only to hold an already saturated rung, there is no definite maximum. It follows that, if several separate windings are present on a hold rung, a current through one or more of them will suffice to hold the rung. For example, in Fig. 5(d) rung 2 could be held by individual currents through separate windings representing A_1, A_2, A_3, $\cdots$, A_n, so that the output would be obtained for inputs satisfying the Boolean equation $F = (A_1 + A_2 + A_3 + \cdots + A_n)BC$. It follows that a single Laddic can be used to generate any Boolean function of the form

$$(X_{11} + X_{12} + \cdots + X_{1n})(X_{21} + \cdots + X_{2n}) \cdots (X_{m1} + \cdots + X_{mn}). \quad (1)$$

Equation (1) is a general form that can represent any Boolean function if the X's may represent either the variables or their negations. In other words, any Boolean function can be generated by a single Laddic if current pulses are available for all of the variables and their negations.

Since a Boolean function can also be written as a sum of products, namely,

$$(X_{11} X_{21} \cdots X_{m1}) + \cdots + (X_{1n} X_{2n} \cdots X_{mn}), \quad (2)$$

it follows that another way to generate the function is to use one Laddic to generate each term in the sum, and connect the output windings in series so that a pulse on any one Laddic appears as an output.

This second procedure can sometimes lead to a considerable simplification of the Laddic circuitry. As an example, consider the alternating symmetric function of four variables, which expresses the condition that an output should be obtained if, and only if, one or three of the four variables are present as inputs. If w, x, y and z represent the four variables, the appropriate Boolean function may be written as follows:

$$= wx'y'z' + w'xy'z' + w'x'yz' + w'x'y'z$$
$$+ wxyz' + wxy'z + wx'yz + w'xyz.$$

This expression can be factorized as follows:

$$F = (w + x + y + z)(w + x + y' + z')(w + x' + y + z')(w + x' + y' + z)$$
$$\cdot (w' + x + y + z')(w' + x + y' + z)(w' + x' + y + z)(w' + x' + y' + z').$$

This is in the form of (1), so that, using the first design procedure, the function could be generated on a single Laddic having eight "held" rungs, with four variable windings on each.

The function can also be rewritten in the following form:

$$F = (w + x)(w' + x')(y' + z)(y + z') + (y + z)(y' + z')(w + x')(w' + x)\cdot$$

Thus, using the second design procedure, the function could be obtained by combining the outputs of two Laddics, each having four "held" rungs with two variable windings on each, as in Fig. 6. In this case, a total of only 16 variable windings is required, compared to the total of 32 needed when using the first method. Thus, the wiring is considerably simplified. It should be noted that when two Laddics are used to generate the variable, as in the present case, the two separate outputs can conveniently be combined in one magnetic circuit, as illustrated in Fig. 7. Thus, the alternating symmetric function of four variables could be generated as conveniently on a single Laddic, using a drive at each end and taking the output from the middle.

Up to the present it has been assumed that current sources are available for both the variables and their negations. Occasionally this may not be practicable. In this connection, it should be noted that terms like

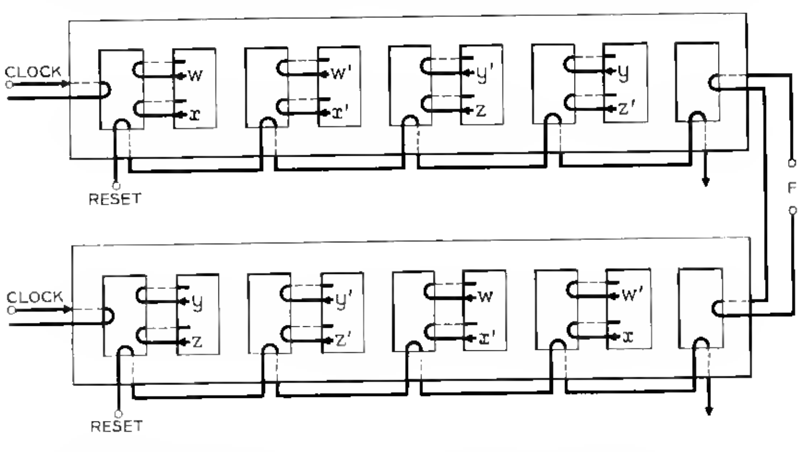

Fig. 6 — Two-Laddic circuit for generating an alternating symmetric function of four variables.

$x(y_1'y_2' \cdots y_n')$ can be produced on a single "held" rung, using currents to represent only the variables but not their primes. The procedure is to apply the x current, which could either represent a variable or be the clock current, in a direction to "hold" the rung. The currents representing the variables y are applied in a direction to counteract the "holding" drive of x, each being sufficient to prevent the rung from being "held". Thus, x will "hold" the rung when y_1 to y_n are absent, but not when one or more of them is present, so that the required Laddic output will be obtained. This procedure can always be applied if the second design procedure, using several Laddics with a common series output, is used, because the Boolean expression (2) can always be reduced to a suitable form. Therefore, it is not essential to have current sources for both a variable and its negation.

4.2 *Modified Procedures*

In Section 4.1 an outline of the basic procedures used in designing Laddic circuits was given. In practice, it is often possible to simplify the circuitry considerably by modifying the drive and output windings. For example, in connection with the alternating symmetric function of four variables it was pointed out that the single Laddic circuit could be simplified by using two drive windings in place of the conventional single drive winding. Since the optimization depends largely on the system requirements, a final design may vary from one application to another. Thus, it is not practicable to list all possibilities; rather, in this section, a number of representative examples will be given.

Using the first design procedure, a single Laddic having a total of n "held" rungs would be required to generate a term of the type

$$(x_1x_2 \cdots x_{n-1})\ (x_n + x_{n+1} + \cdots + x_m);$$

that is, n-1 "held" rungs for the first term $(x_1 \cdots x_{n-1})$ and one "held" rung for the second term $(x_n + \cdots + x_m)$. The same function can be gen-

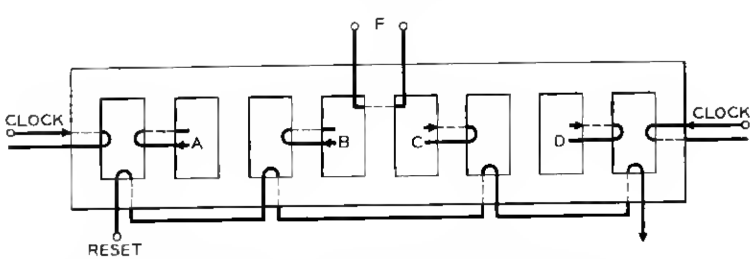

Fig. 7 — Illustrating use of a more complicated drive winding; $F = AB + CD$

erated using the four-rung Laddic shown in Fig. 8. In this, the primes of the variables x_1 to x_{n-1} are all used in opposition to the clock drive to prevent it from switching at all, and the variables x_n to x_m are used to "hold" rung 2. The result is a considerable shortening of the Laddic required, and therefore a proportionately faster switching speed for a given drive. Of course, there is no reduction of the total number of windings necessary.

Occasionally, both the function and its negation are required. The negation may be taken from the same Laddic by using an output winding which links flux changes in all rungs except the first and output rungs. Thus, an output will occur on this winding if and only if no pulse occurs on the output winding. In some cases, it may even be simpler to generate a function by using the Laddic to generate its negation according to the customary method, and to take the output from the negation winding.

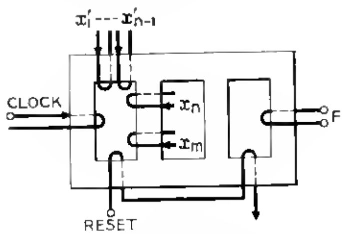

Fig. 8 — Modified Laddic circuit; $F=(x_1\ x_2 \cdots x_{n-1})\ (\ x_n + x_{n+1} + \cdots + x_m)$

For example, in order to generate $F = x_1'x_2' + x_2x_3' + x_1'x_3'$, using the conventional output winding, the Laddic circuit shown in Fig. 9(a) is required. Using the negation winding, the simpler circuit shown in Fig. 9(b) can be used. The use of more complicated output windings of this nature is not generally recommended because the switching speeds will vary with the return path, so that the output amplitudes will differ for the different combinations of inputs. This is not the case using the conventional output. In addition, the signal-to-noise ratio is usually worsened, because of the possibility of undesired coupling. If the output requirements are not rigorous, output circuits of this kind can be satisfactory, but generally the conventional output is preferred.

A different mode of operation is based upon the following observation. If a short-circuited winding is placed around an even-numbered variable rung, for example, rung 2, 4, or 6 in Fig. 5(d), an output is obtained from the winding on the next available rung, e.g., rung 8 in Fig. 5(d). This occurs because, as flux attempts to switch through a "shorted" rung, the emf induced in the winding produces a current which opposes the applied switching drive in exactly the same manner as the hold currents do in

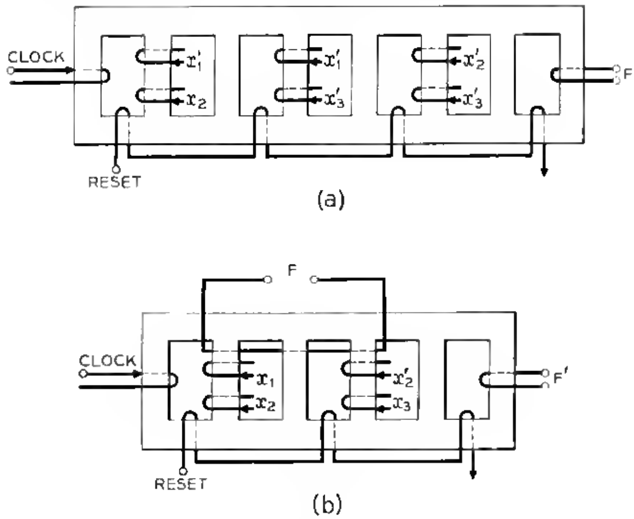

Fig. 9 — Laddic circuits illustrating the use of a negation output winding; $F = x_1'x_2' + x_1'x_3' + x_2 x_3' = (x_1' + x_2)(x_1' + x_3')(x_2' + x_3')$; $F' = x_1 x_2' + x_1 x_3 + x_2 x_3 = (x_1 + x_2)(x_2' + x_3)$.

the normal mode. However, if a suitable opposing emf is introduced in the shorted winding, no current will flow, so that the flux can switch through the rung and there will be no output. The opposing emf can represent an input variable. In other words, an output will be obtained when the input variables are absent. Thus, the operation is almost an exact dual to the normal mode, with the constant current sources representing variables being replaced by constant voltage sources. In practice, a rung will not be entirely "held" by the self-induced current, because the short-circuited winding will have a finite resistance. Thus, not all of the flux will be returned through the output rung, and there will be a small attenuation of the output signal.

In all of the examples up to now, the switching drive during the variable input phase has been considered to be a clock drive, and has not represented a variable input. In some applications this is an advantage, because the "hold" currents representing variables are never required to switch flux, provided that the flux pattern is reset during a subsequent reset phase, so that quite low impedance sources may be used. Furthermore, the timing of the variable pulses is not critical, the only restriction being that they be applied before or at the same time as the clock pulse, and remain at least until the end of the switching period. For other applications, these considerations may be unimportant and, in this case,

windings which represent any one of the factors in (1), may replace the normal clock winding on rung 1.

4.3 *Modified Structures*

It will be apparent from the previous section that the Laddic structure makes a very versatile circuit element. For specific applications, an economy in size and windings can sometimes be obtained by using a more complicated, less general structure in place of the Laddic. Broadly speaking, these alternative structures may be based upon the following operating principles as used in the Laddic:

i. The structure has a number of stable flux patterns.

ii. A normal or original flux pattern is set up in this structure.

iii. The tendency of this pattern to change to other fixed flux patterns according to the presence or absence of various applied fields is utilized to determine the actual switching path through the structure.

It is not the purpose of this paper to outline a design procedure for producing an optimum structure. Instead, one elementary example will be given. In Fig. 10(a) is shown the conventional Laddic circuit for generating the function $x(z + wy)$. Because both rungs 2 and 4 can be held by variable z, it follows that this part of the magnetic circuit

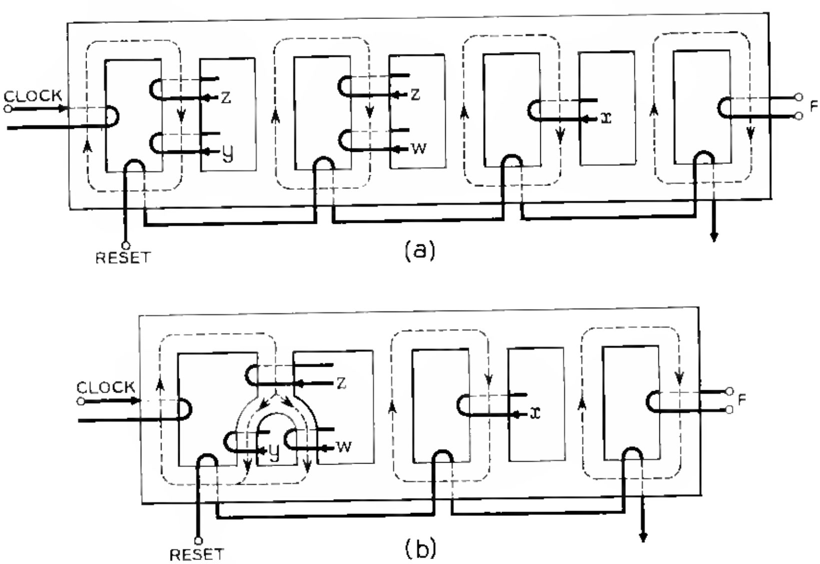

Fig. 10 — Simple illustration of the use of a more complicated structure; $F = x(z + wy)$. The main features of the reset flux pattern are shown.

can be combined as shown in the modified structure of Fig. 10(b). It will be noticed that the cross sections of the split rungs carrying variables y and w are shown as one-half of that carrying variable z in order to preserve a saturated flux structure. This modified structure has one less variable winding, and may be shorter than the conventional Laddic circuit.

In the Laddic structure, no use is normally made of the odd-numbered rungs except for the first. These rungs serve only to maintain flux continuity in the particular flux patterns used. The same result could be achieved by combining them elsewhere in the magnetic circuit, at the same time enlarging the side rails to maintain flux continuity, as in Fig. 11, for example. In Fig. 11 the rungs 1, 2, 4, 6, 8 and 10 are labelled to correspond to the like rungs of the Laddic, Fig. 5, and the remaining odd-numbered rungs are considered to be collected together on the left-hand side of rung 1 to provide the flux returns for the reset flux pattern as illustrated. Operation would then be as in the Laddic, the flux in rung 1 being reversed by the clock drive, rungs 2, 4, 6 and 8, being "held" by variable inputs, and an output being taken off rung 10.

It might be thought that this structure would give a gain in switching speed because the distance between rung 1 and rung 10 is reduced. However, experimentally the switching speed is found to be characterized by a switching path length such as $ABCD$, rather than the shorter path $abcd$. The distance aA is approximately equal to the sum of the widths of the intermediate rungs. Thus, there is little actual gain in switching speed. More serious is the fact that the flux limiting action of the side rails is reduced, and the signal-to-noise ratio degenerates. Accordingly, the conventional Laddic structure is considered preferable.

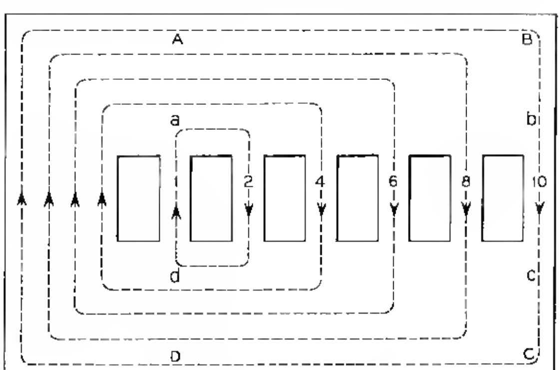

Fig. 11 — Modified Laddic structure.

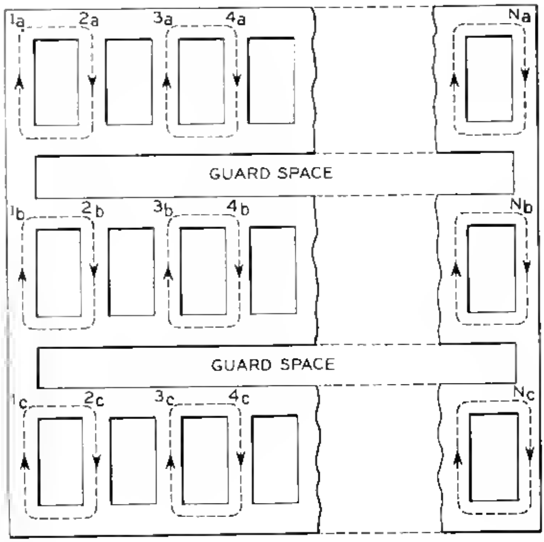

Fig. 12 — Combination of Laddics on a single sheet. The normal reset flux pattern is shown.

Another advantage of the Laddic structure is that it is compact laterally, so that it is practicable to combine several adjacent Laddics on a continuous sheet, as illustrated in Fig. 12. The guard spaces shown are sufficient to prevent any interaction between the adjacent Laddics.

4.4 *Cascading Laddics*

There is never any necessity for cascading Laddics for combinational logic, since the desired result can always be realized using single Laddic circuitry. In fact, the latter is inherently more efficient, because a cascade circuit must provide additional power to allow for dissipation in the coupling loops. A cascade circuit can produce some simplification in cases where the output of one Laddic can provide a common input for a number of others. The design problems here are reasonably straightforward and need no discussion.

In the following, two methods for coupling Laddics for sequential operation will be described.

The first method is illustrated in Fig. 13. The output of the first Laddic is used to provide the switching drive for the second. During phase Φ_1, the first Laddic is "set" by its input variables, and the second Laddic is reset. During phase Φ_2, the second Laddic is set, the first Laddic being simultaneously reset to provide the appropriate advance current. Clearly

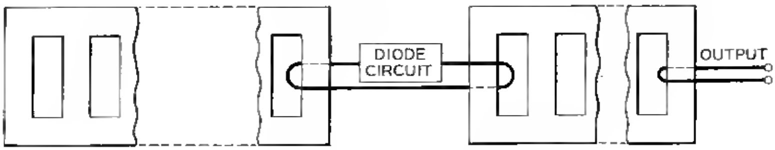

Fig. 13 — First method for cascading Laddics.

the intermediate "hold" rungs play a secondary part only in the advance operation, since they are not included in the coupled switching path. Thus, when considering the advance operation, the Laddic may be treated as a conventional core of the same peripheral length. It follows that Laddics may replace cores in conventional core circuits for sequential operation, and that an intermediate diode circuit or a transistor is necessary to prevent back propagation.[5] Because additional logical inputs may be inserted at each stage of the cascade, the Laddic circuit can be more versatile than the corresponding core circuit.

A second possibility for coupling Laddics is illustrated in Fig. 14. In this case, the output of the first Laddic is used to provide the hold current for a rung of the second Laddic. As before, the clock phase Φ_1 of the first Laddic coincides with the reset phase of the second, and *vice versa* for Φ_2. This procedure appears promising at first sight because there need be no diode in the coupling loop. Furthermore, a high coupling efficiency might be anticipated, because the advance current is not required to switch flux in the held rung of the second Laddic, and so the back emf is small. However, the coupling efficiency is actually limited, because a resistance must be included in the coupling loop. Otherwise, as discussed in Section 4.2, the loop would act as a short-circuited turn

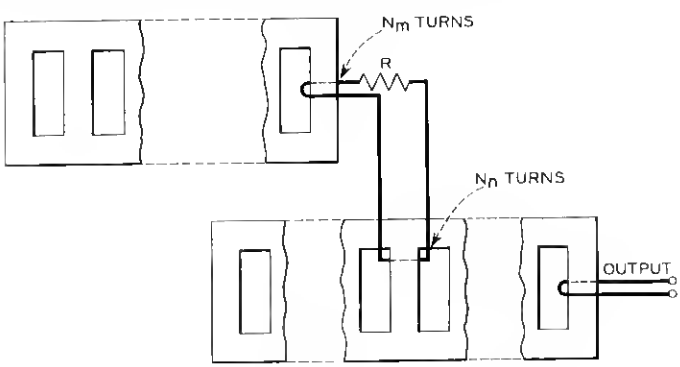

Fig. 14 — Second method for cascading Laddics.

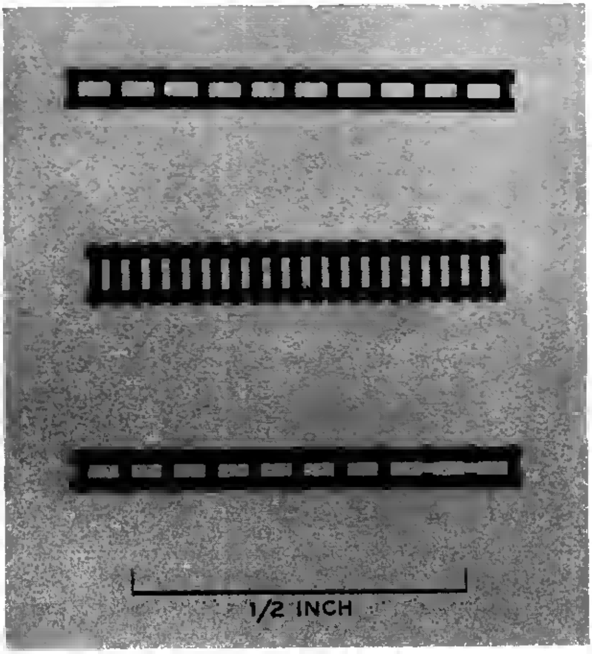

Fig. 15 — Photograph of experimental Laddics.

and hold the coupled rung of the second Laddic even when there is no output from the first Laddic, thus making the output of the second Laddic independent of the first. To allow for the power dissipated in R the turns ratio Nm/Nn in the coupling loop must exceed unity. A detailed analysis has shown that these requirements are necessarily different for each stage of the cascade, becoming more rigorous with each successive stage. It is considered that a two-stage diodeless cascade is the only case worthy of practical consideration.

V. EXPERIMENTAL RESULTS AND DESIGN FORMULAE

5.1 *Experimental Laddics*

For experimental purposes, Laddics are cut out of a ferrite sheet, using an ultrasonic cutter. Fig. 15 illustrates the size of Laddics which have been used. The smallest unit was made from a sheet of cadmium manganese ferrite 30 mils thick, the width of the rungs and side rails being 15 mils, the spacing between rungs 15 mils and the spacing between side rails 50 mils. In order to improve the signal-to-noise ratio,

the output window is sometimes enlarged by cutting out some of the rungs as in one of the units shown in Fig. 15. The actual dimensions used were chosen somewhat arbitrarily, keeping in mind the convenience of fabrication and handling. As will be shown later, from the point of view of minimizing drives for a given switching speed, the over-all length should be as small as possible. When used with single turn windings, the units shown can be driven by a transistor pulser. The output for a given drive—that is, for a given switching speed—is approximately proportional to the cross section of the rung (A cm^2), and to the remanent flux density (B_r gauss) of the material. For an output waveform approximately rectangular in shape, the mean output voltage per turn E is $E \cong B_r A \times 10^{-8}/\tau$ volts, where τ is the switching time in seconds. For the experimental units, $B_r A \cong 5.8$ and a normal range for τ was 1 to 5 microseconds.

The requirements on the structure and material are not very stringent. The best signal-to-noise ratios are obtained with close dimensional control, although a relative dimensional tolerance of 5 per cent is found to be adequate in practice. For the same reason, the material should be homogeneous and have a good squareness ratio B_r/B_s . The best material from the point of view of minimizing drives has a low threshold field for switching, H_0 , and a small switching time constant, s. From the point of view of maximizing the output, B_r should be as large as possible

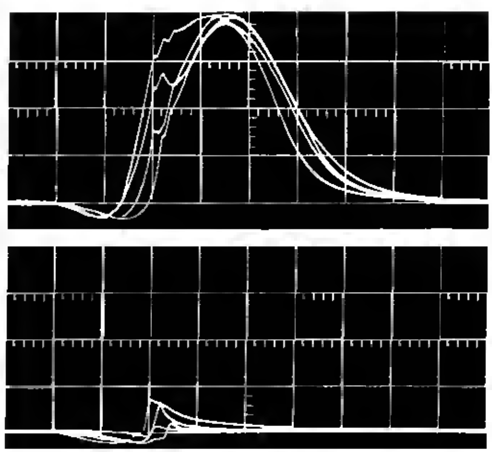

Fig. 16 — Signal and noise outputs for the circuit shown in Fig. 17. The vertical calibration is 0.01 volt/turn/large division. The horizontal calibration is 1 μs/large division. The variable currents were all equal and equal to the clock current, which was 0.8 ampere. Single-turn windings were used.

In practice, available memory core ferrites for which $B_r \cong 2400$ gauss, $H_0 \cong 0.17$ oersted, $B_r/B_s \cong 0.92$, and $s \cong 0.8$ oersted microsecond are reasonably satisfactory.

Representative output waveforms are shown in Fig. 16, which is discussed in the next section in connection with Fig. 17.

The important parameters of the Laddic are the values of the minimum currents needed to hold the variable rungs and the switching speed, for a given drive, switching path and material. Useful design formulae are derived in the following sections.

5.2 *Hold Currents*

As discussed previously, the hold currents necessary to prevent flux from being switched in the corresponding rungs must exceed a certain minimum. This minimum is proportional to, and obviously less than, the switching drive current, and decreases with the distance between the held rung and the driven rung. The following simple treatment gives a relation between the minimum hold currents, drive current and switching path, which agrees satisfactorily with experiment. These assumptions are made:

i. During switching the amount of flux by-passed from the desired switching path by the held rungs and the saturated rungs of the Laddic is negligible.

ii. The reluctance of the side rails, and of the input and output rungs, is linearly proportional to their length.

iii. The concepts of static magnetic circuitry can be applied to the dynamic switching problem for the particular problem considered here.

The first assumption can be justified because there is a difference of at least two orders of magnitude between the relative permeabilities of switching and nonswitching paths in a rectangular loop material. The second assumption can be only a first-order approximation, because the reset flux pattern is such that the initial reluctance of a side rail may

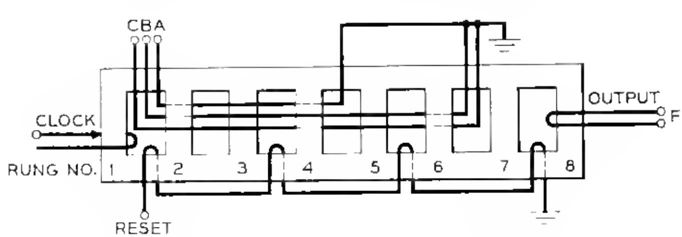

Fig. 17 — Experimental Laddic circuit; $F = (A + B)(A + C)(B + C)$.

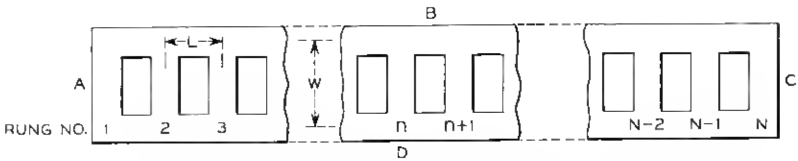

Fig. 18 — Diagram to show peripheral lengths referred to in the text.

not be uniform along its length. The justification for the third assumption is that it has been shown to be useful in a previous study of a dynamic magnetic circuit.[6]

Let L be the mean length per window of the Laddic, and let W be the mean width, Fig. 18. Let a switching mmf M_1 be applied to rung 1, and let holding mmf's $M_2, M_4, \cdots M_n, \cdots M_{N-2}$, which exactly balance the switching mmf's appearing across them, be applied to the even-numbered rungs 2 to $(N - 2)$, inclusive. Thus the switching flux return is through rung N. In this case, according to assumptions i, ii and iii, the ratio M_n/M_1 will be equal to the ratio of the reluctance or length of the portion of switching path BCD beyond rung n to the total switching path $ABCDA$, Fig. 18. Thus,

$$\frac{M_n}{M_1} = \frac{BCD}{ABCDA} = \frac{W + 2(N - n)L}{2W + 2(N - 1)L} = \frac{N - n + W/2L}{N - 1 + W/L}, \tag{3}$$

For the smallest Laddic dimensions shown in Fig. 15, $W \cong 2L$, and M_n/M_1 is tabulated for this case in Table II.

Experimentally, the minimum hold drives $(M_n)_{\text{exp}}$ necessary to operate the Laddic were determined by adjusting the holding currents to the minimum values necessary to produce maximum switching of flux in rung N, when a switching drive was applied to rung 1. The ratios M_n/M_1

Table II — Ratios of Minimum Hold Drive M_n to Clock Drive M_1 for the Case $W = 2L$.

N	n = 2	4	6	8	10	12	14
4	0.60						
6	0.71	0.43					
8	0.78	0.56	0.33				
10	0.82	0.64	0.46	0.27			
12	0.85	0.69	0.54	0.38	0.23		
14	0.87	0.73	0.60	0.47	0.33	0.20	
16	0.88	0.76	0.65	0.53	0.41	0.29	0.18

were measured for all of the input-output conditions covered by Table II, and for two typical values of the rung 1 drive, $M_1 = 0.3$ ampere turn, and $M_1 = 0.65$ ampere turn. Experimental accuracy was about ± 10 per cent. It was found that the experimental ratios agreed with the predicted values to within ± 15 per cent. When comparing the experimental and predicted values, it was assumed that $(M_n)_{\text{exp}}$ was equal to $M_n - M_c$, where M_c is the effective bias mmf in the rung due to the coercive field of the material. For the present case, $H_c \cong 0.17$ oersted, and rung length is 50 mils, so that $M_c \cong 0.02$ ampere turns.

It is concluded that (3) is an adequate representation for design purposes.

5.3 *Signal-to-Noise-Ratio*

In principle, there is no upper limit to the hold currents. However, the signal-to-noise ratio degenerates with increasing hold currents because of lack of squareness of the *B-H* loop, the noise signal corresponding to the zero output of a memory core. The noise pulse decreases as the distance of a hold drive from the output winding increases, and in the Laddic only the final stages of the hold currents are serious sources of noise. An extreme practical case occurs when the hold currents are all equal to the first. Table II shows that, in this case, the final hold current is more than five times its minimum value in the 16-rung Laddic. Fig. 19(a) shows the signal and noise outputs that were obtained experimentally, using a 16-rung Laddic, for the condition where all of the hold currents are at their minimum values, as defined by (3). The remaining outputs shown were those obtained as a progressively increasing number of hold currents were made equal to the minimum value for rung 2, leaving the remainder at their previous values. The noise signal shown was the maximum that could be obtained, that is, when M_2 alone was missing. Single-turn windings were used throughout. It will be seen that the signal-to-noise ratio is excellent when all hold currents are at their minimum values, Fig. 19(a), but that the noise signal deteriorates as an increasing number of hold drives are made equal to M_1. However, for many applications, the signal-to-noise ratio is tolerable even for the extreme case of all hold currents equal. If necessary, the ratio may be improved by enlarging the effective size of the output window, as in the modified Laddic shown in Fig. 15, or by permanently holding the final rungs by means of direct currents through the hold windings. Both methods have been shown experimentally to reduce the influence of the hold currents on the output noise signal.

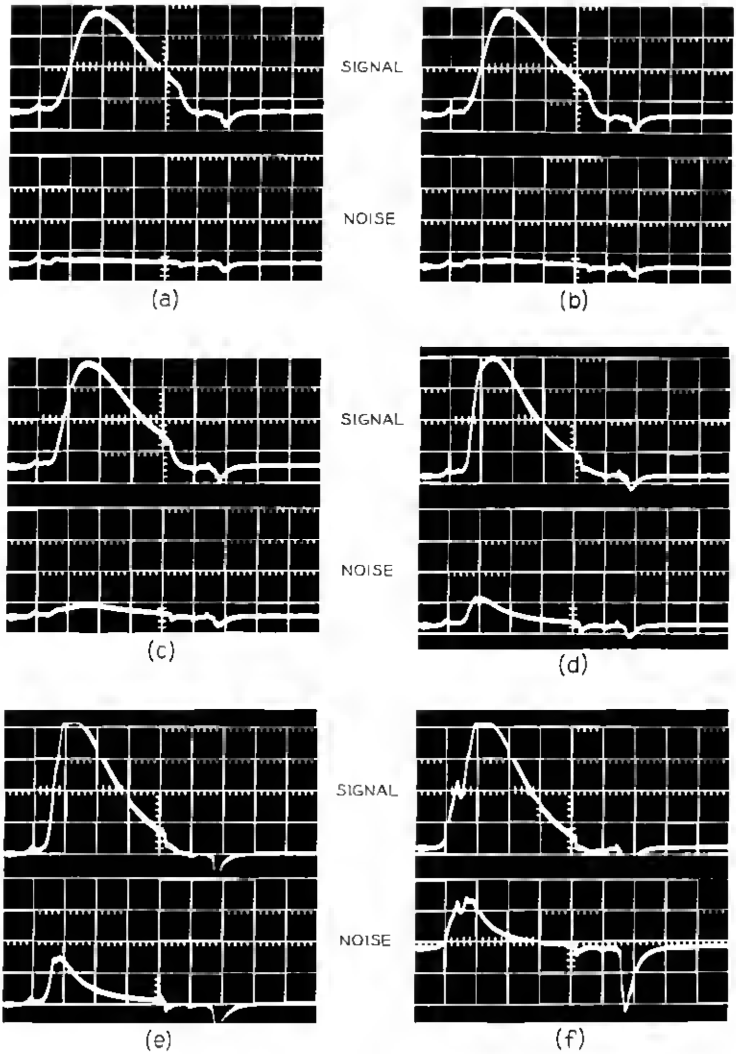

Fig. 19 — Signal and noise outputs taken from the sixteenth rung of a Laddic showing the effect of increasing the hold currents beyond their minimum values, (a) all hold currents at their minimum values; (b) M_2, M_8, M_{10}, M_{12}, and M_{14} at their minimum values, remaining hold currents equal to M_2; (c) M_2, M_{10}, M_{12} and M_{14} at their minimum values, remaining hold currents equal to M_2; (d) M_2, M_{12} and M_{14} at their minimum values, remaining hold currents equal to M_2; (e) M_2 and M_{14} at their minimum values, remaining hold currents equal to M_2; (f) all hold currents equal to M_2.

An illustrative case of practical interest, where equal hold currents must be used, is that of producing the carry (K) of a full binary addi-

tion. In Boolean algebra notation, $K = AB + AC + BC$. This can also be written in the form $K = (A + B)(A + C)(B + C)$. This function can be produced by the Laddic circuit shown in Fig. 17. In this circuit, rung 2 is held by $(A + B)$, rung 4 by $(A + C)$ and rung 6 by $(B + C)$, so that an output results only if two or three of the input variables are simultaneously present. If single-turn windings are to be used, all the hold currents are necessarily approximately equal. The outputs that were obtained experimentally for the separate inputs, ABC', $AB'C$, $A'BC$ and ABC, are shown superimposed in Fig. 16(a). The outputs obtained for the remaining possible inputs, $A'B'C'$, $A'B'C$, $A'BC'$ and $AB'C'$, are shown superimposed in Fig. 16(b). It is clear that, even when all the hold currents are equal, the signal-to-noise ratio is adequate for most purposes. Thus, apart from satisfying the condition for the minimum hold current, the margin requirements are lax.

The foregoing discussion is based on the assumption that the Laddic structure is uniform in geometry and material. If this is not the case, the reset flux pattern may be affected and, as a result, irreversible flux changes may contribute to the noise pulse. This contribution will only be large when the available flux from the hold rungs cannot be entirely returned by rungs other than the output rung. This condition can be avoided by making the odd-numbered rungs large enough and/or providing a bias winding which links odd-numbered rungs to ensure more complete saturation of all rungs.

A complete description of Laddic noise is complicated and will not be attempted here. It should be remarked that, in many circuits, no special noise suppression techniques appear to be necessary.

5.4 *Switching Speed*

The convention[7] will be adopted here that the switching time be measured between the points of 10 per cent of maximum amplitude of the output waveform.

If it is assumed, as in the last section, that the rungs of the Laddic may be ignored unless they are included in a switching path, then, for the purpose of determining switching speeds, the Laddic may be treated as a memory core of the same peripheral length. The length of the switching path when the output is taken off rung N is equal to $2(N - 1)L + 2W$, Fig. 18. Thus, since the switching time τ is related to the applied drive by the usual relation,[7] $\tau(H - H_0) = s$, for the Laddic

$$\frac{1}{\tau} = \frac{1}{s}\left[\frac{0.2\pi M_1}{W + (N - 1)L} - H_0\right]; \tag{4}$$

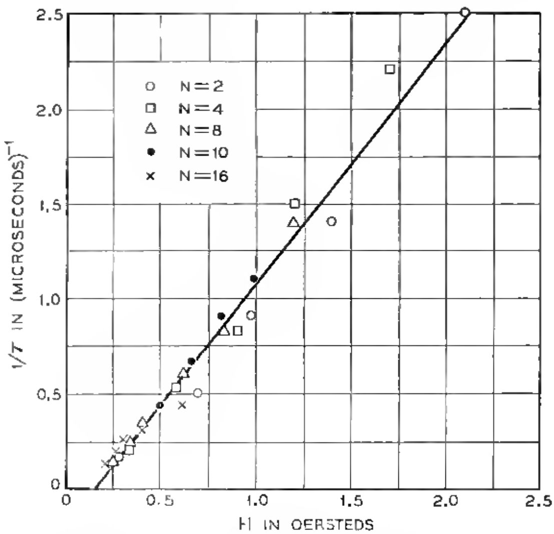

Fig. 20 — Experimental plot of inverse switching speed versus applied field, $H = (0.2\pi M_1)/[W + (N - 1)L]$, for outputs taken from the 2nd, 4th, 8th, 10th and 16th ring of the Laddic.

M_1 is in ampere turns, W and L in centimeters, H_0 in oersteds and s in oersted microseconds.

The experimental relations for the 20 hole Laddic shown in Fig. 15, ($W = 2L$), are shown in Fig. 20, for N in the range 2 to 16. It is concluded that (4) is a satisfactory representation. The values of s and H_0, derived from Fig. 20, are $s = 0.77$ oersted microsecond and $H_0 = 0.15$ oersted.

It should be remarked that, for these measurements, all the hold currents were maintained at their minimum values. If this is not the case, the output waveforms may be modified, and the effective switching times may change. However, the data presented give the approximate magnitudes.

5.5 *Impedances*

Since the hold current is not called upon to switch flux, the impedance of a hold winding is quite small. It is equal to $r + j\omega l$, where r is the resistance of the winding, and l its inductance. For a single-turn winding typical values are $r \sim 0.02$ ohm, $l \sim 0.01$ microhenry.

The impedances for the clock and reset drives are approximately resistive and may be derived from the usual core formula.[8]

5.6 *Cascading*

Two methods for cascading Laddics were described in Section 4.4. The first method was shown to be similar to the cascading of conventional cores, and so need not be considered further. As stated, the second method has limited applicability, but it is still of practical interest. For this reason the characteristics of a two-stage cascade will be described.

Refer to Fig. 14. Approximate relations for the minimum values of R and N_m/N_n are the following:

$$R_{\min} = \frac{4\pi\varphi_r N_n^{\,2}}{s(L_{10} - L_{1n})}, \tag{5}$$

$$\left[\frac{N_m}{N_n}\right]_{\min} = \frac{L_{1m}}{L_{10}}\frac{R}{R_{\min}}. \tag{6}$$

In deriving (5) and (6) it was assumed, as a first-order approximation, that the rate of change of flux $\dot{\varphi}$ is constant during the switching period. Equations (3) and (4) were used for the minimum hold currents and switching speeds respectively; L_{1m} and L_{10} are the mean peripheral lengths of the first and second Laddics, i.e., $ABCDA$ in Fig. 18, and L_{1n} corresponds to the peripheral length DAB; φ_r is the total flux available for switching, and was assumed to be equal in the two Laddics; R is the actual loop resistance. All units are in cgs.

Equations (5) and (6) have been found to provide a reasonable guide to practical design. As an example, consider the circuit shown in Fig. 21. For $N_n = 1$ the theoretical $R_{\min}$ is 0.2 ohm. Experimental output wave-

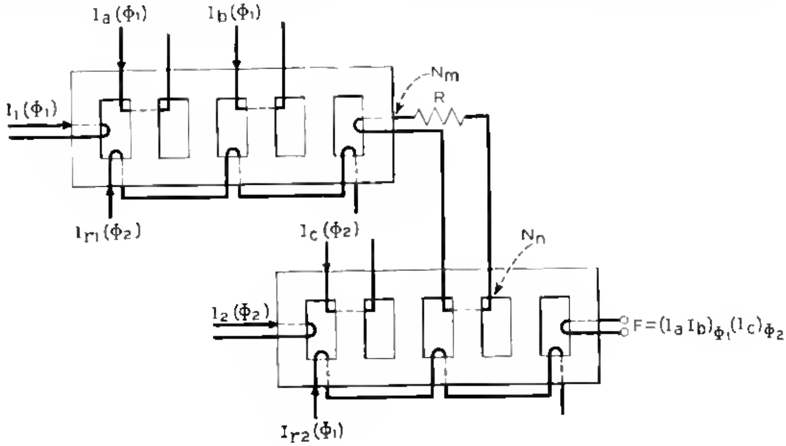

Fig. 21 — A two-Laddic cascade.

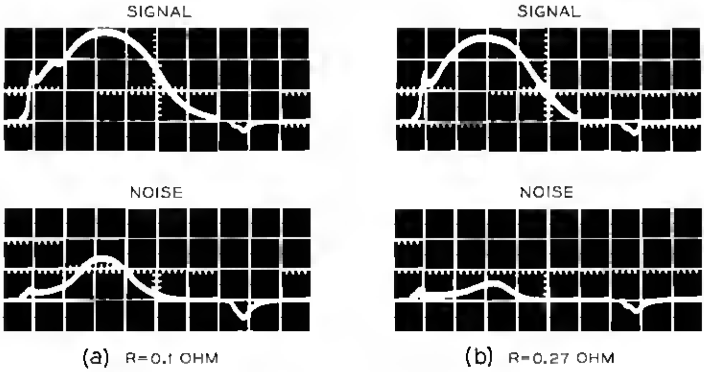

Fig. 22 — Experimental waveforms from the circuit of Fig. 21, with $N_m = 4$.

forms for one value of R on either side of $R_{\min}$, $N_n = 1$ and $N_m = 4$, are shown in Fig. 22. It will be seen that, as R is increased through the theoretical minimum, the main effect is to decrease the amplitude of the "0" signal, as is to be expected.

For a given N_m/N_n and R, the ratio of the current drives I_{r1}/I_2 must exceed a certain minimum to provide an adequate advance hold current; I_{r1}/I_2 also has a maximum limit, for otherwise the advance hold current will not persist for the full switching period of the second Laddic. The margin between maximum and minimum vanishes if N_m/N_n is equal to or less than the theoretical minimum. In practice, R should be chosen close to $R_{\min}$, and N_m/N_n made as large as practicable. Table III illustrates the maximum and minimum current ratios obtained experimentally using the circuit of Fig. 21, for different parametric values. It will be seen that, for a suitable choice of R and N_m/N_n, the operating margins are broad.

Table III — Ratios of Maximum and Minimum Drive Currents for Different Experimental Conditions

N_2I_2 ampere-turns	N_m turns	N_n turns	R ohms	$(I_{r1}/I_2)_{\min}$	$(I_{r1}/I_2)_{\max}$
0.3	6	1	0.43	2.8	>4
0.3	6	1	0.26	3.0	>4
0.3	6	1	0.1	3.0	>4
0.3	4	1	0.42	2.0	3.0
0.3	4	1	0.25	2.0	4.0
0.3	4	1	0.1	2.0	>4
0.3	2	1	0.1	min. and max. overlap	

VI. DISCUSSION

The Laddic structure is a versatile one for use in logic circuitry. More complicated structures, as discussed, may offer particular advantages when certain functions have to be realized, but for many applications the Laddic structure is sufficient.

The details of Laddic behavior are not yet completely understood. Their understanding probably requires a more thorough explanation of the switching process in ferrites. However, by making a number of simple assumptions it has been possible to give simple formulae and design techniques for Laddic circuits, which appear in general to be satisfactory.

The Laddic is basically a device for combinational logic and, as shown, a single Laddic can be used to realize any switching function of n variables. For systems applications where sequential operation is necessary, it may be used in conjunction with intermediate diode or transistor circuitry. In certain cases, the intermediate circuitry is not necessary.

The Laddic is a simple device to make. Suitable materials are available, and their properties are not very critical, provided that the material is reasonably homogeneous. For experimental purposes these devices have been cut out of solid ferrite sheets, but for larger scale fabrication the green ferrite would more conveniently be pressed into the final form. Experience with other ferrite devices suggests that pressing into the final form will slightly improve the material properties. Because of the use of single-turn windings for the variables, the wiring of a Laddic is fairly simple. It involves dropping a hairpin-shaped conductor across a rung, and a number of simple assembly schemes can be thought of. The reset winding is more complicated, because it involves threading a number of holes with a single wire. Printed wiring is very suitable for this purpose.

The speed of the Laddic is basically the same as that of other magnetic core devices, being limited primarily by the properties of available materials. Switching speeds of a few tenths of a microsecond and repetition rates of a few hundred kilocycles have been achieved. For many applications in the telephone system, speed is not a prime requirement.

No attempt will be made in this paper to compare Laddic circuits with conventional core logic circuits, or with other multi-aperture devices. A useful comparison would be one that covered all possible applications, and this is not practicable. The main merits of the Laddic are its probable low cost, versatility and compatibility with existing core circuits, and the convenience of its design from the point of view of fabrication.

VII. ACKNOWLEDGMENTS

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